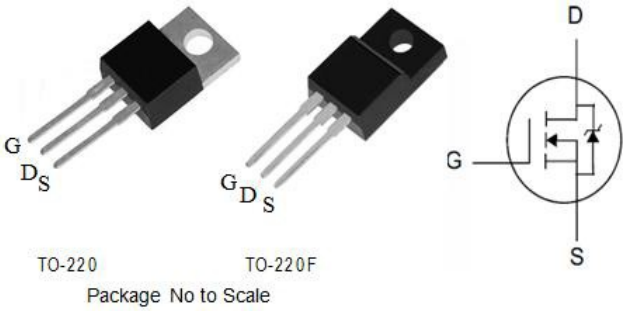
650V N-Channel Planar MOSFET

Lead Free Package and Finish

Features

- 10A,650V,$R_{DS(ON),typ.}$=0.80 Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- 100% Avalanche Tested
- RoHS Product



Package No to Scale

Applications

- Adaptor
- Charger
- SMPS Standby Power

Absolute Maximum Ratings (TC = 25 °C unless otherwise noted)

Symbol	Parameter	JMF10N65C	JMA10N65C	Units
V_{DSS}	Drain-Source Voltage	650		V
V_{GSS}	Gate-Source Voltage	±30		
I_D	Continuous Drain Current	10		A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	40		
E_{AS}	Single Pulse Avalanche Energy	800		mJ
P_D	Power Dissipation	125	45	W
	Derating Factor above 25℃	1.0	0.36	W/℃
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300		℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 ~ 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	JMF10N65C	JMA10N65C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.0	2.78	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	100	

Electrical Characteristics

OFF Characteristics(TC = 25 °C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=650V, V_{GS}=0V
		--	--	100		V_{DS}=520V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics(TC = 25 °C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.80	1.00	Ω	V_{GS}=10V, I_D=5.0A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance	--	8.0	--	S	V_{DS}=15V,ID=5.0A

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	1660	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	15	--		
C_{oss}	Output Capacitance	--	130	--		
Q_g	Total Gate Charge	--	32	--	nC	V_{DD}=520V, I_D=10A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	8.0	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	8.5	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$td_{(ON)}$	Turn-on Delay Time	--	11	--	nS	V_{DD}=325V, I_D=10A, V_{GS}=10V Rg=4.7Ω
t_{rise}	Rise Time	--	15	--		
$td_{(OFF)}$	Turn-Off Delay Time	--	40	--		
t_{fall}	Fall Time	--	17	--		

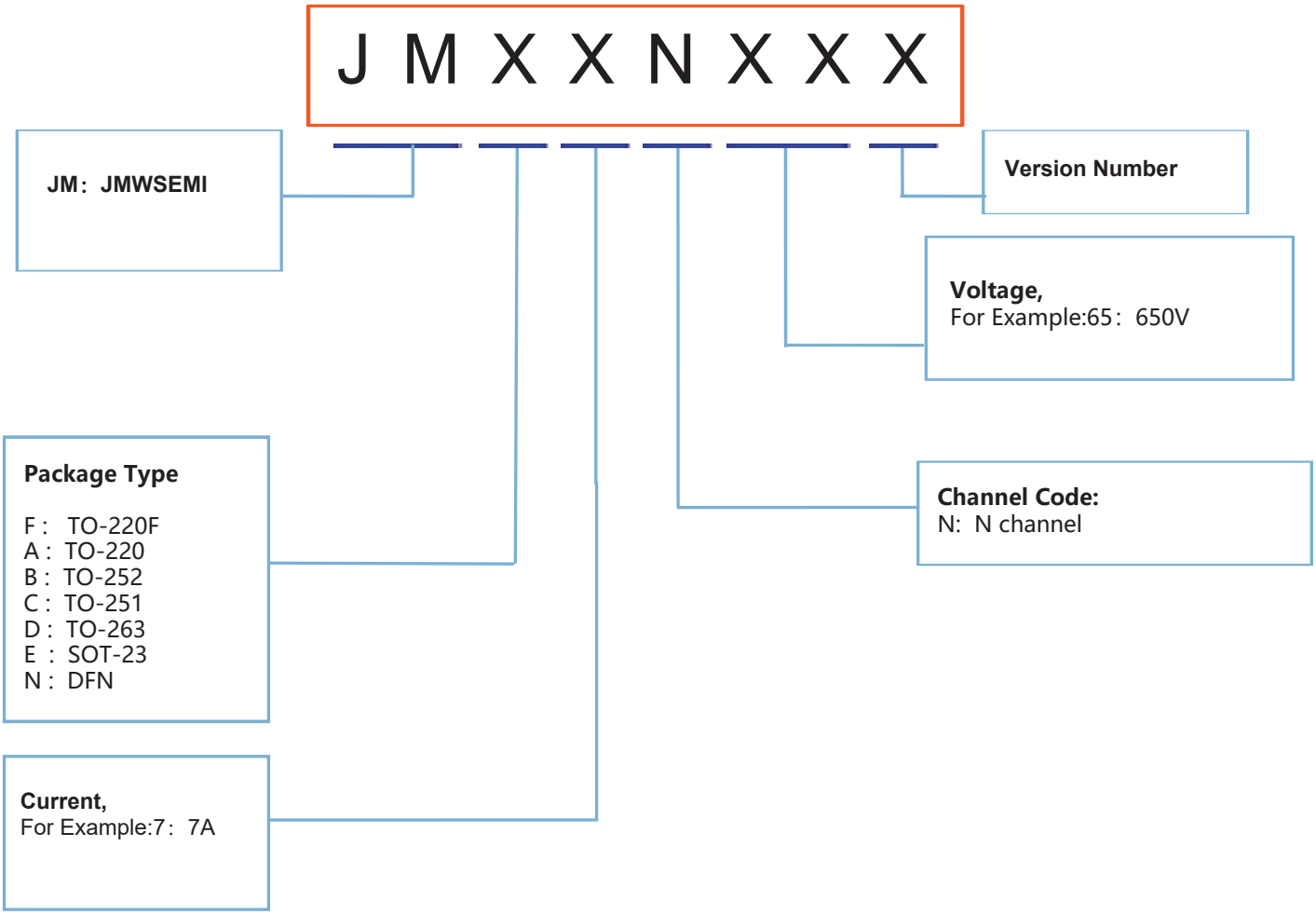
Source-Drain Body Diode Characteristics (TC = 25 °C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	10	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	40		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=10A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	460	--	ns	V_{GS}=0V I_F= I_S, di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	1.5	--	nC	

Note:

[1] TJ=+25°C ~ +150°C
[2] Pulse width≤380μs; duty cycle≤2%.

VD MOS Product Names Rules



Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

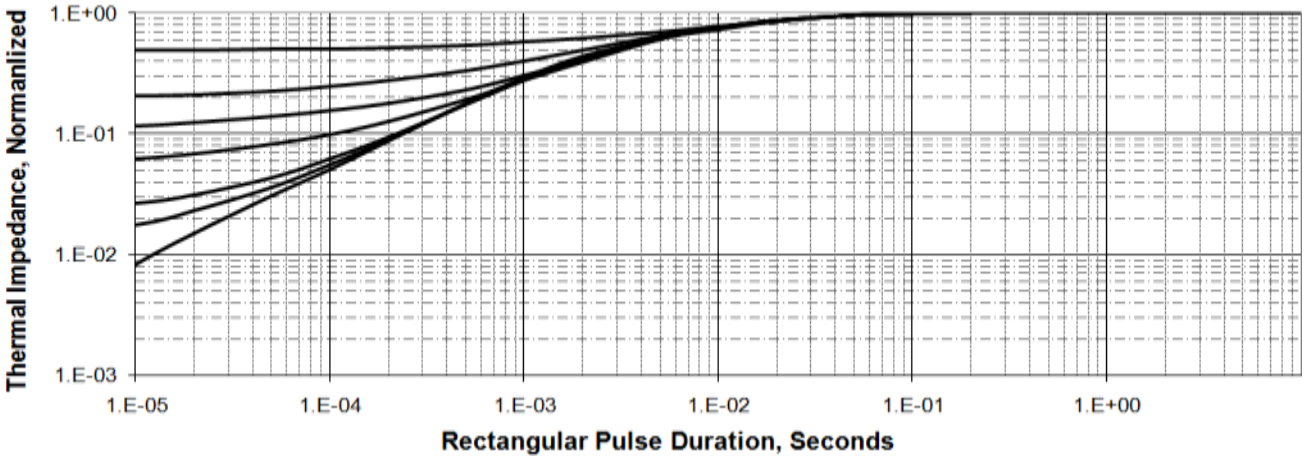


Figure 2 . Max. Power Dissipation vs Case Temperature

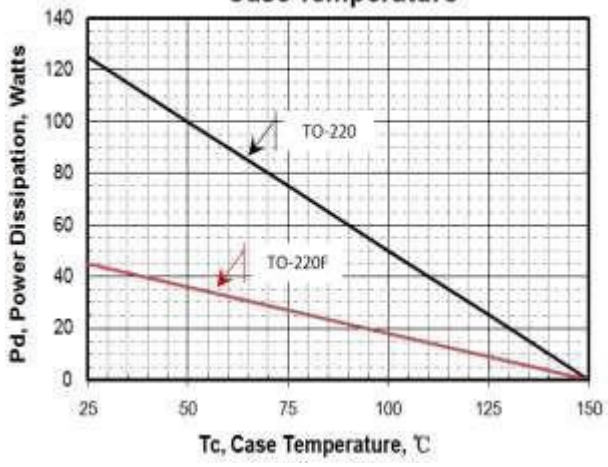


Figure 3 .Maximum Continuous Drain Current vs Tc

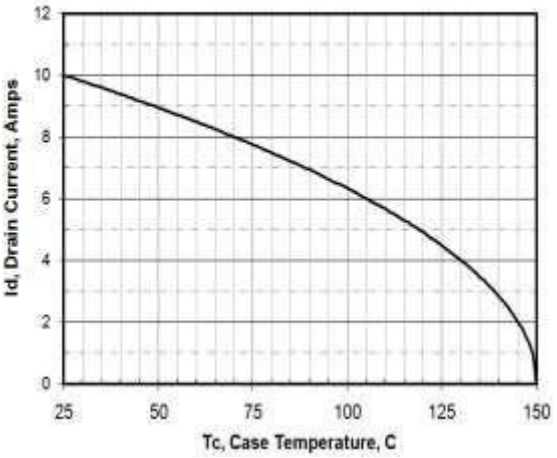


Figure 4. Output Characteristics

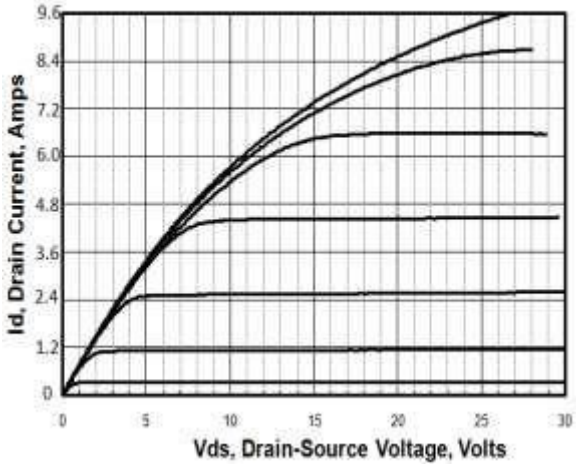
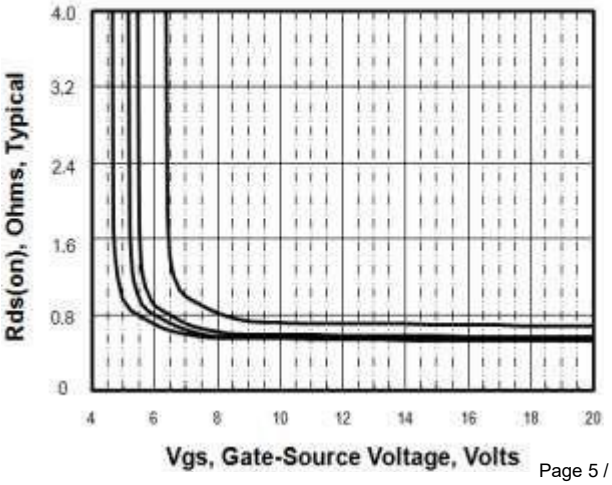


Figure 5. Rdson vs Gate Voltage



Typical Characteristics(Cont.)

Figure 6. Peak Current Capability

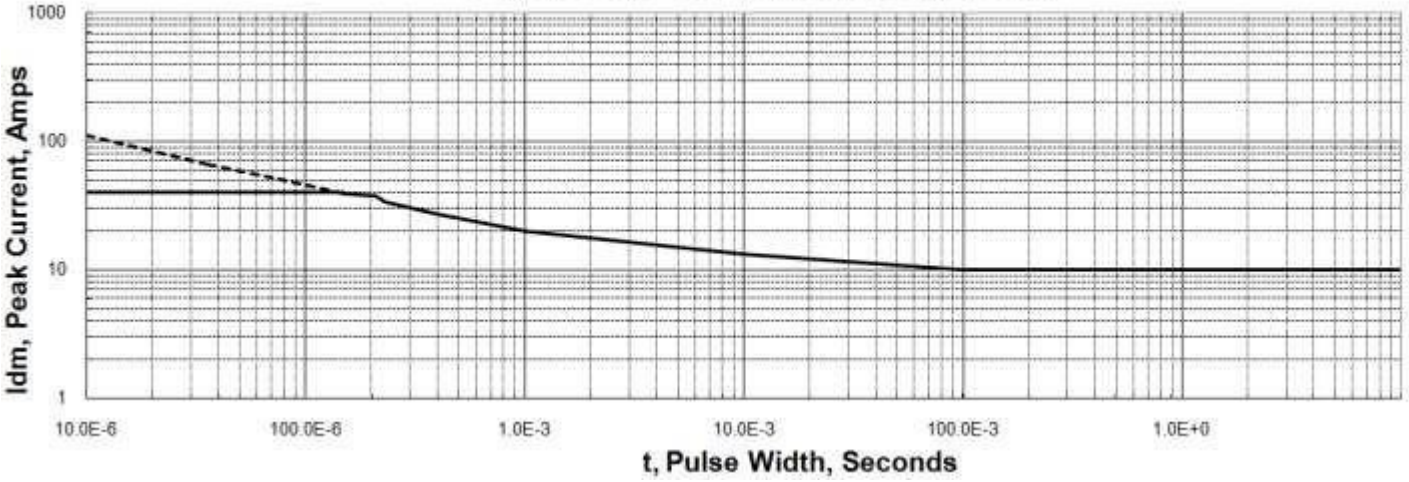


Figure 7. Transfer Characteristics

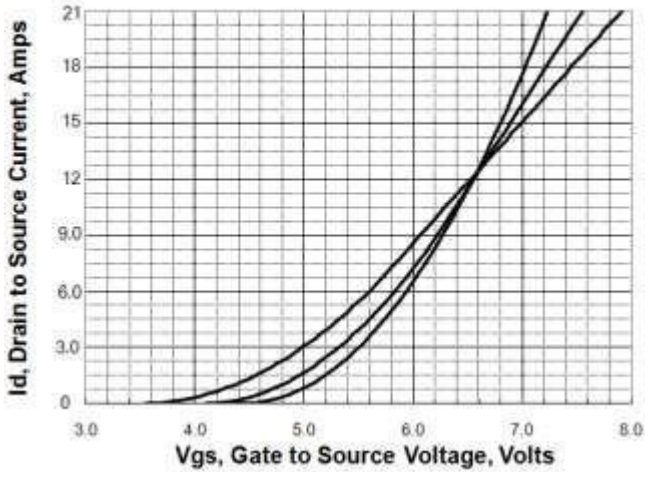


Figure 8. Unclamped Inductive Switching Capability

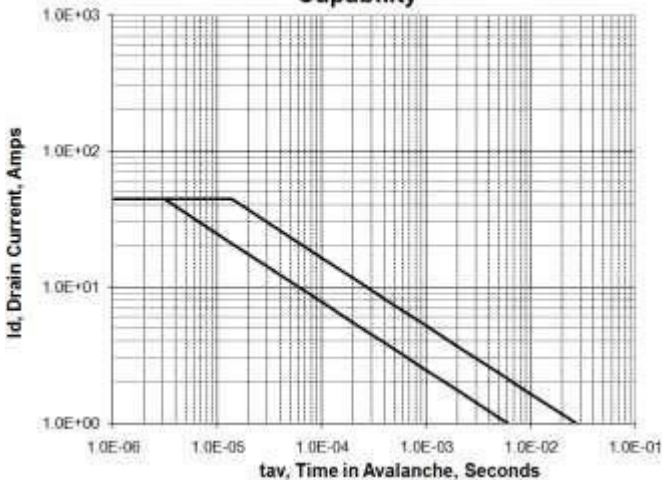


Figure 9. Drain to Source ON Resistance vs Drain Current

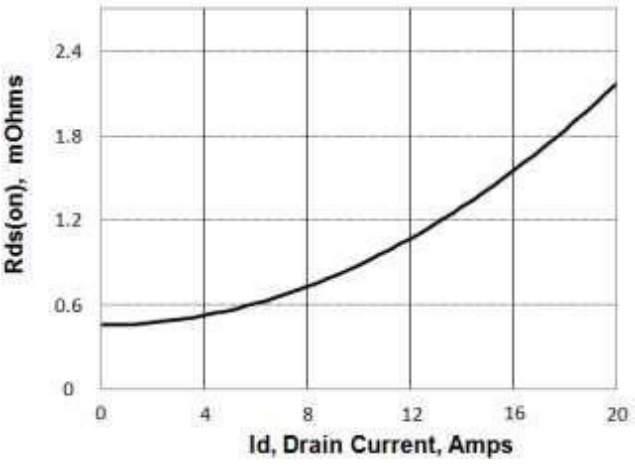
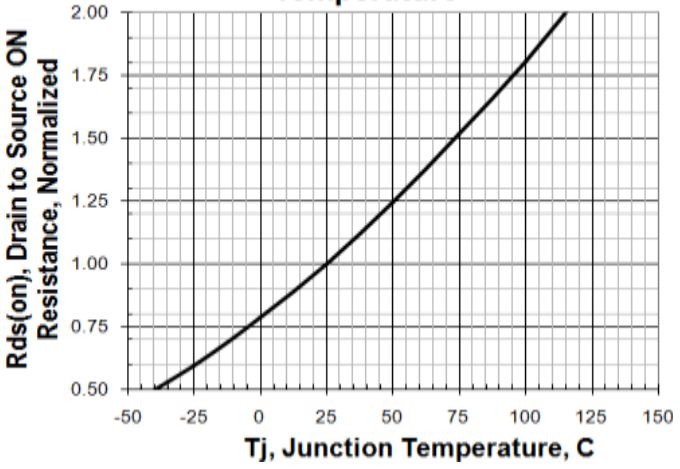


Figure 10. Rdson vs Junction Temperature



Typical Characteristics(Cont.)

Figure 11.Breakdown Voltage vs Temperature

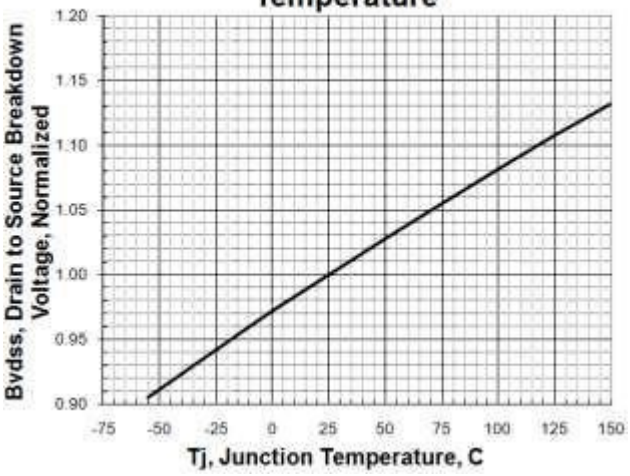


Figure 12.Threshold Voltage vs Temperature

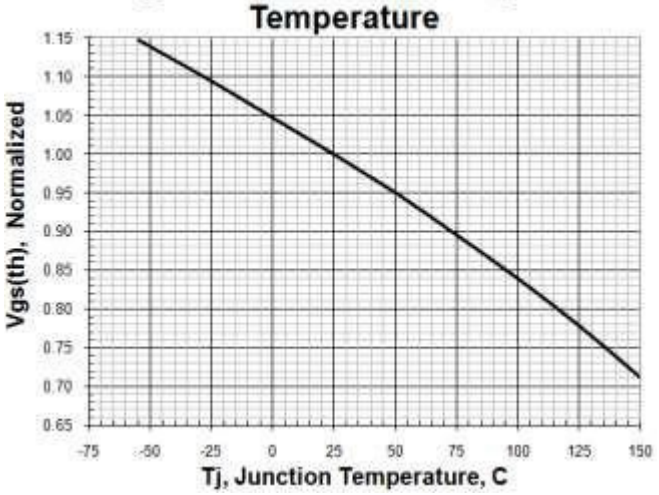


Figure 13 . Maximum Safe Operating Area

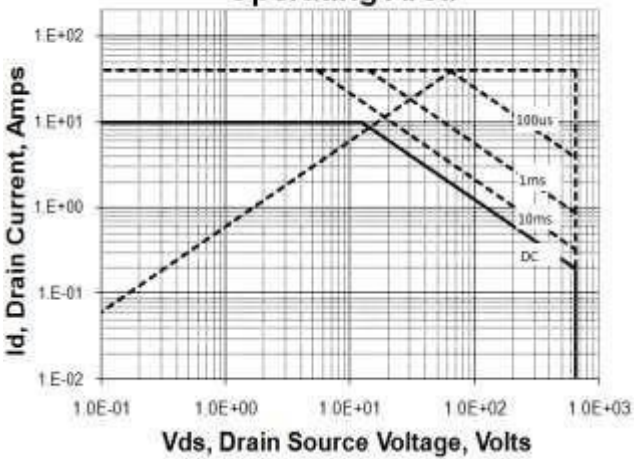


Figure 14. Capacitance vs Vds

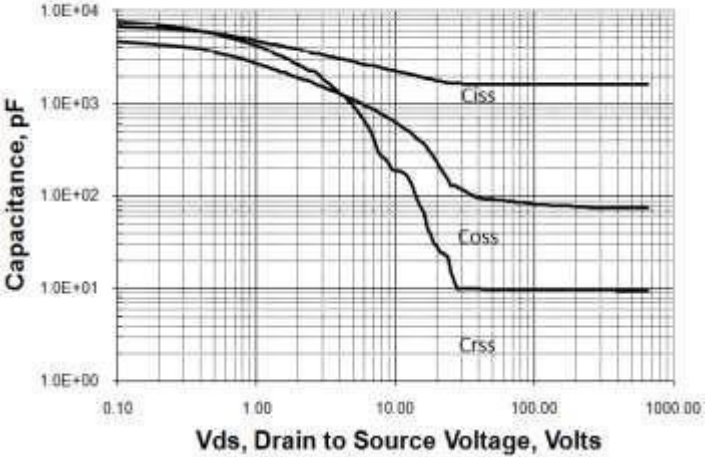


Figure 15 .Typical Gate Charge

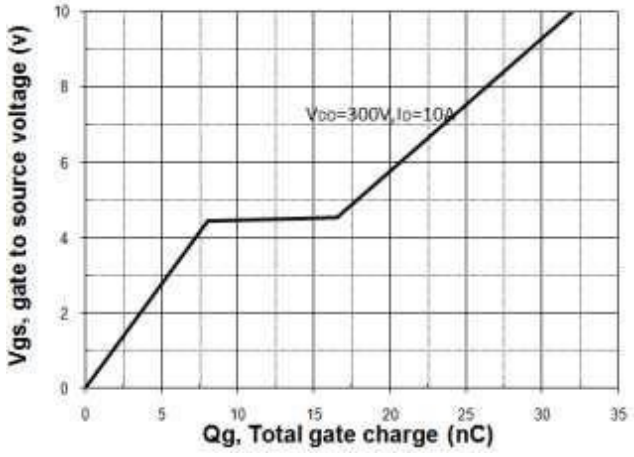
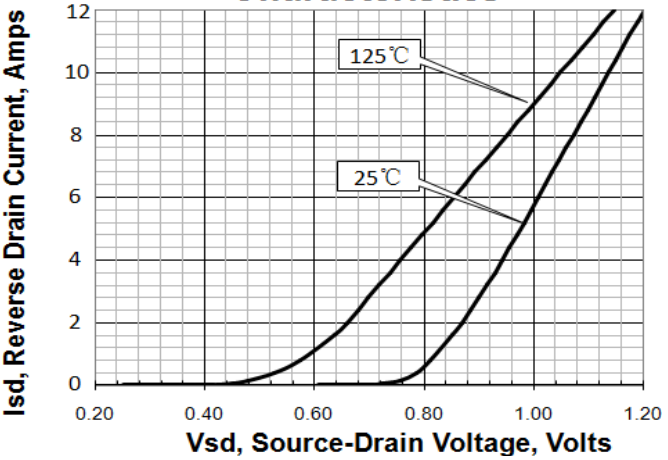


Figure 16.Body Diode Transfer Characteristics



Test Circuits and Waveforms

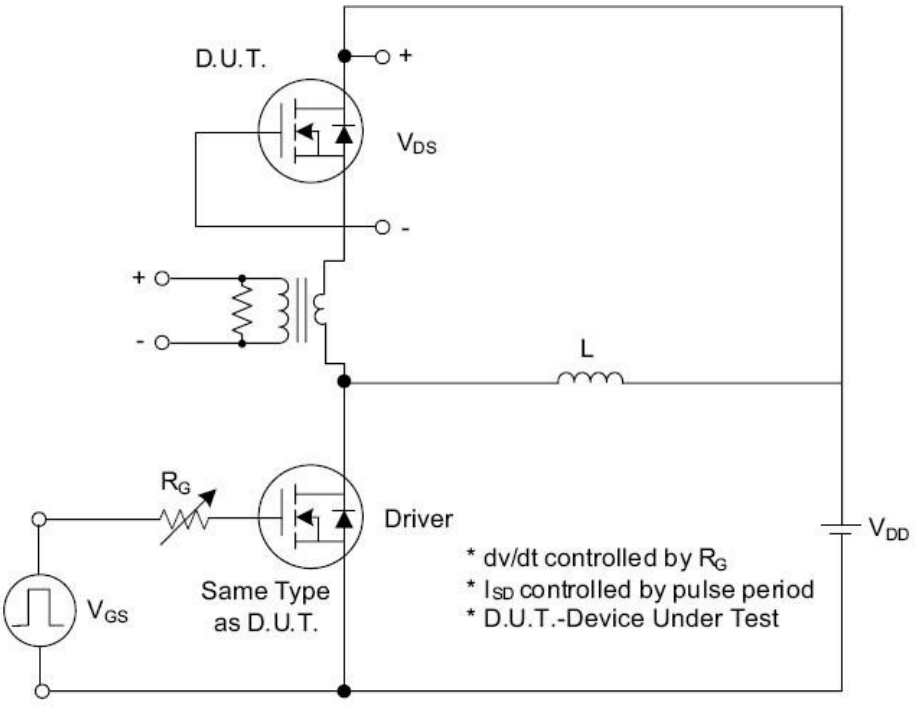


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

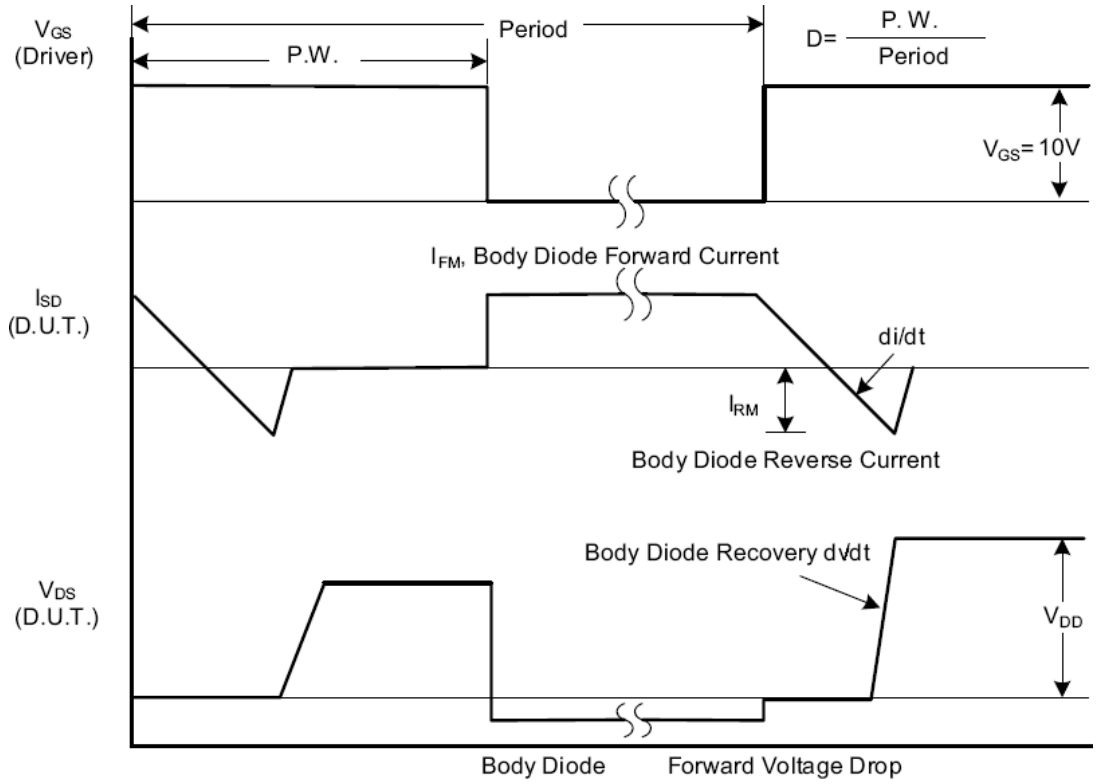


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

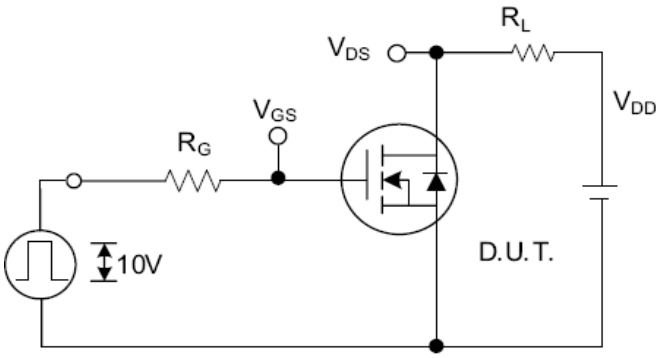


Fig. 2.1 Switching Test Circuit

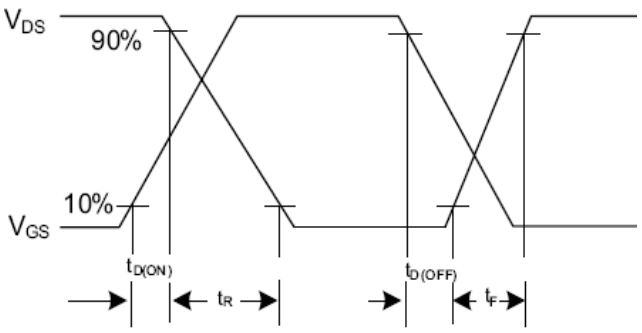


Fig. 2.2 Switching Waveforms

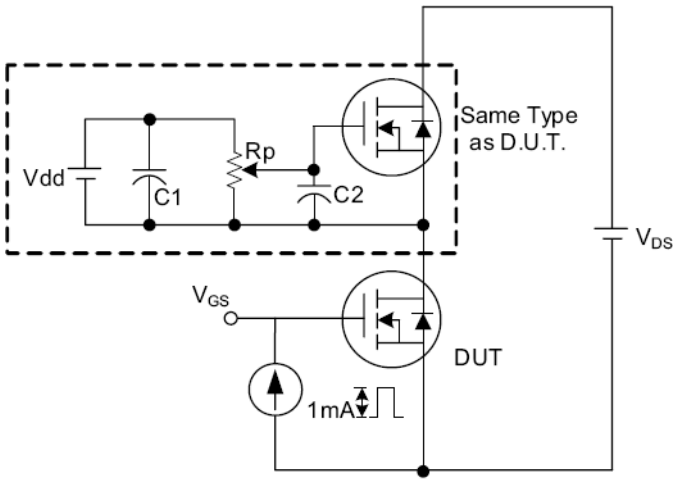


Fig. 3 . 1 Gate Charge Test Circuit

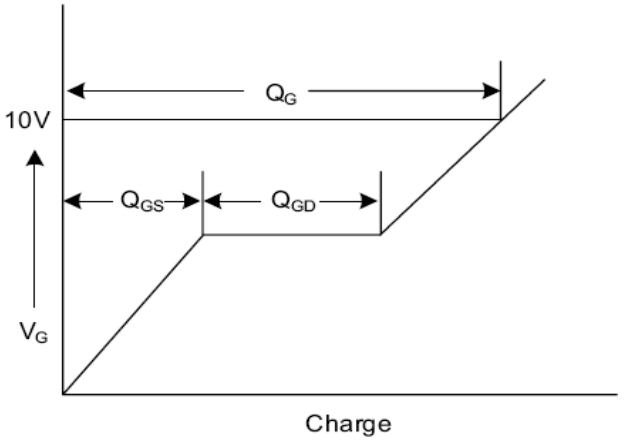


Fig. 3 . 2 Gate Charge Waveform

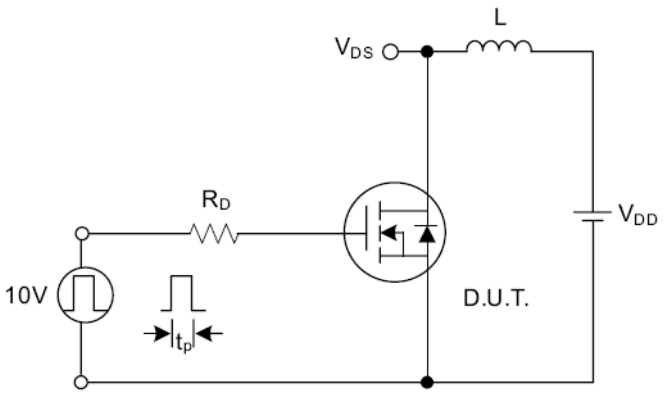


Fig. 4.1 Unclamped Inductive Switching Test Circuit

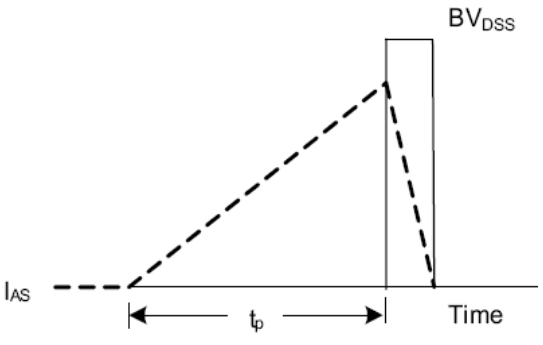


Fig. 4.2 Unclamped Inductive Switching Waveforms

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