

General Features

- Super Low Gate Charge
- Green Device Available
- Provide Excellent RDS(ON)
- Advanced high cell density Trench technology

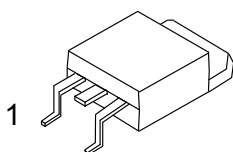
Product Summary



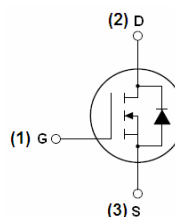
V _{DS}	40	V
R _{DS(on)} ,Max.@V _{GS} =10V	7.5	mΩ
I _D	60	A

Application

- Load Switch
- PWM applications
- Synchronous Buck Converter Applications



TO-252



N-channel

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	40	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	60	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	45	A
I _{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	76.1	mJ
I _{AS}	Avalanche Current	39	A
P _D @T _C =25°C	Total Power Dissipation ⁴	44.6	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient (Steady State) ¹	---	62	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	2.8	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.034	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=12A$	---	---	7.5	$m\Omega$
		$V_{GS}=4.5V, I_D=10A$	---	---	10	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.96	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=12A$	---	39	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	1.6	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=12A$	---	18.8		nC
Q_{gs}	Gate-Source Charge		---	4.7		
Q_{gd}	Gate-Drain Charge		---	8.2		
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=1A$	---	14.3		ns
T_r	Rise Time		---	2.6		
$T_{d(off)}$	Turn-Off Delay Time		---	77		
T_f	Fall Time		---	4.8		
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	2332		pF
C_{oss}	Output Capacitance		---	193		
C_{rss}	Reverse Transfer Capacitance		---	138		

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	60	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	120	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=39A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

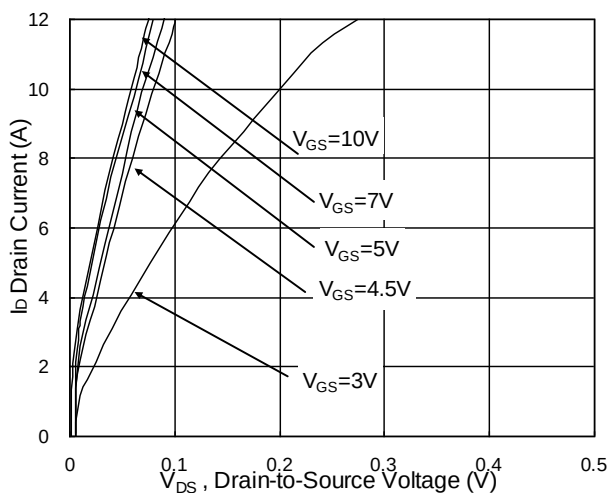


Fig.1 Typical Output Characteristics

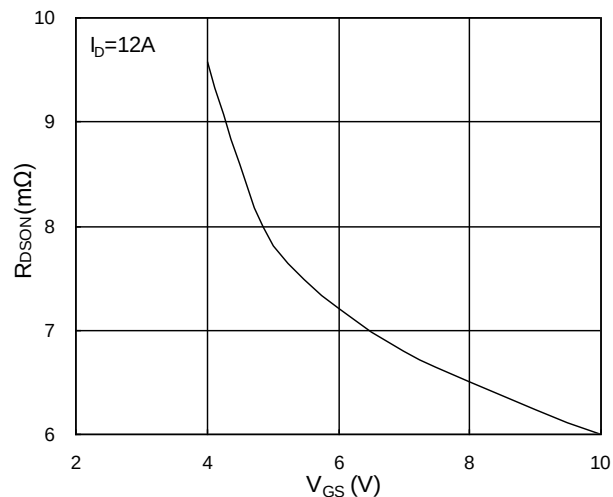


Fig.2 On-Resistance vs. G-S Voltage

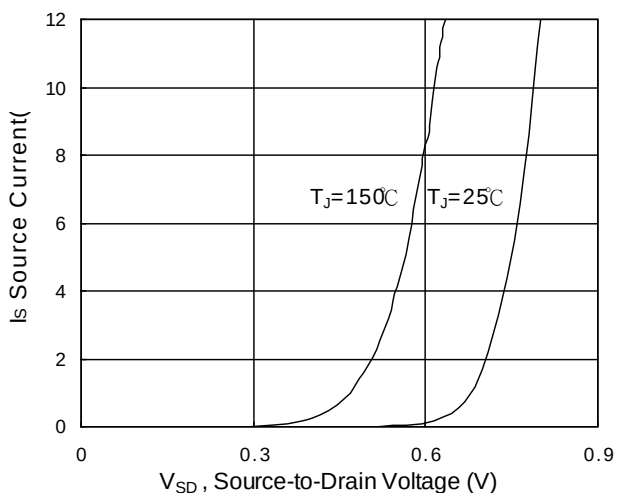


Fig.3 Forward Characteristics of Reverse

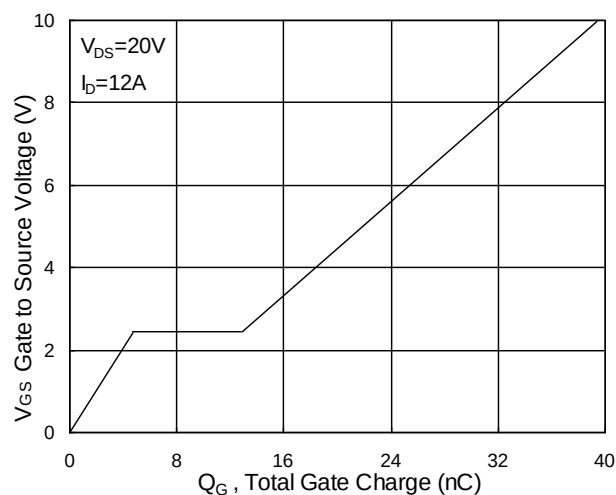


Fig.4 Gate-Charge Characteristics

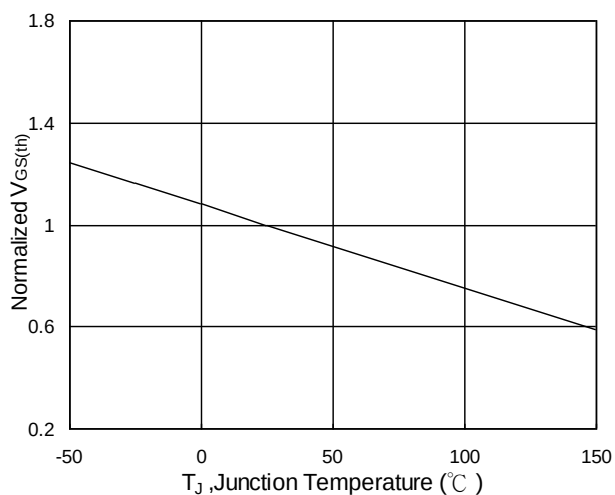


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

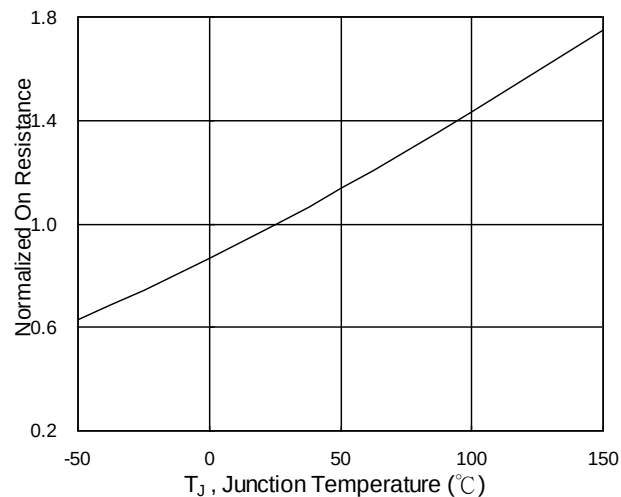


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

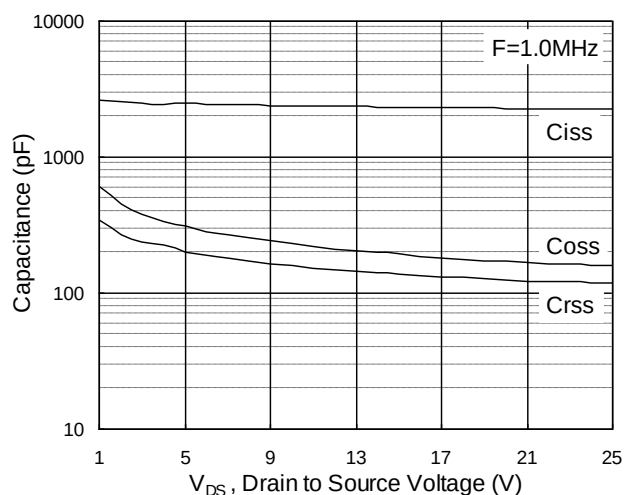


Fig.7 Capacitance

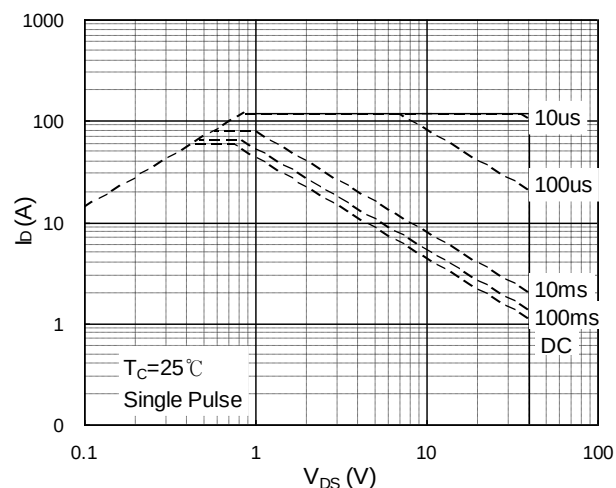


Fig.8 Safe Operating Area

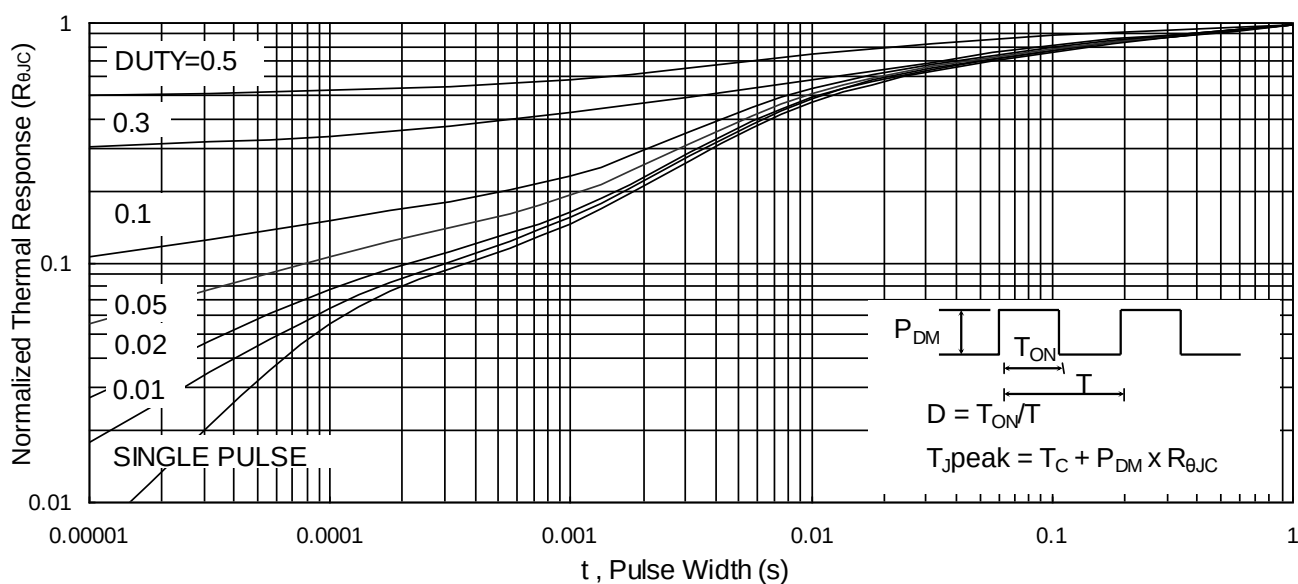


Fig.9 Normalized Maximum Transient Thermal Impedance

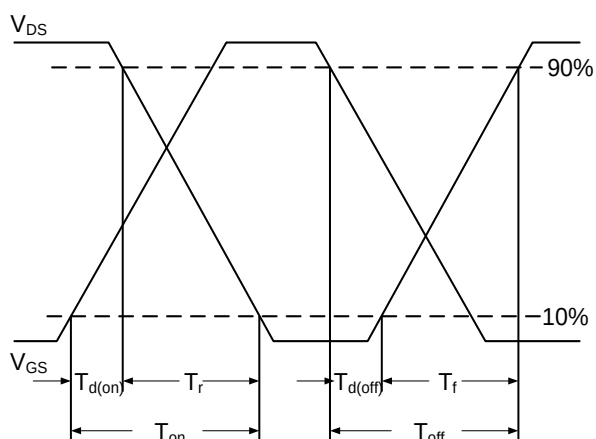


Fig.10 Switching Time Waveform

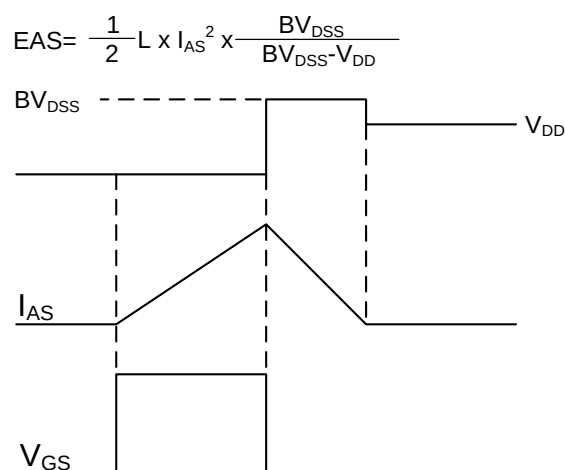


Fig.11 Unclamped Inductive Waveform

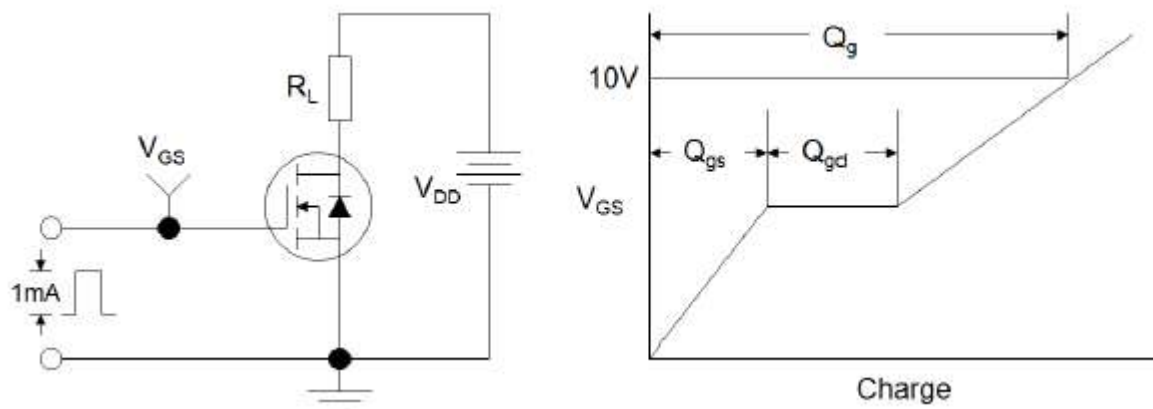


Figure1:Gate Charge Test Circuit & Waveform

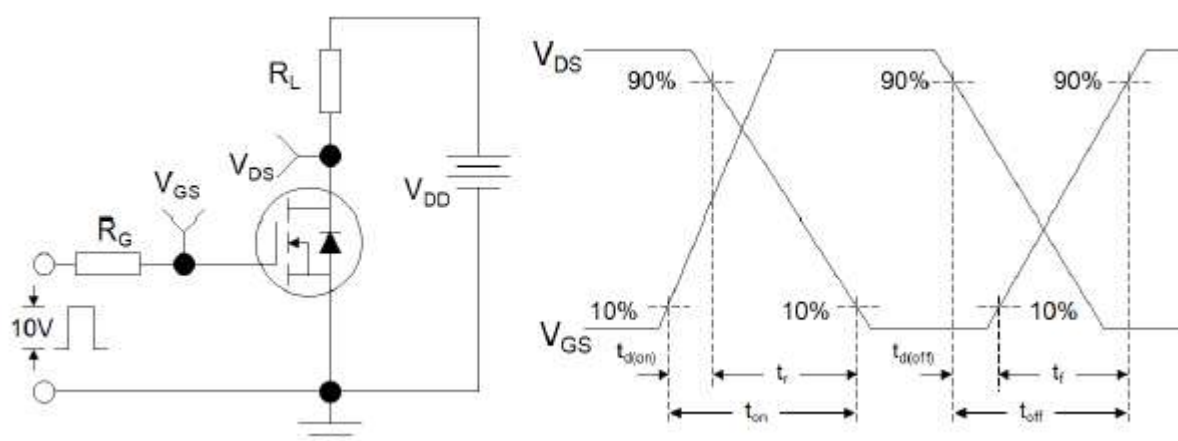


Figure 2: Resistive Switching Test Circuit & Waveforms

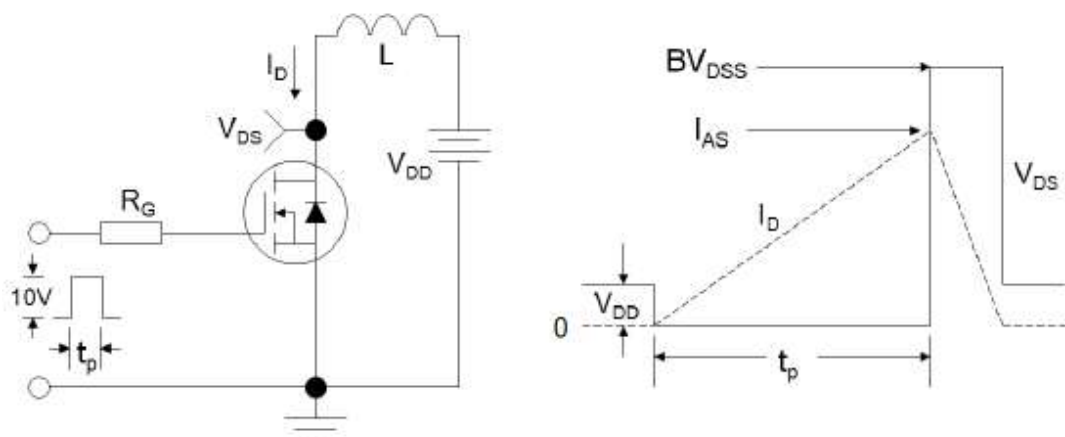


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

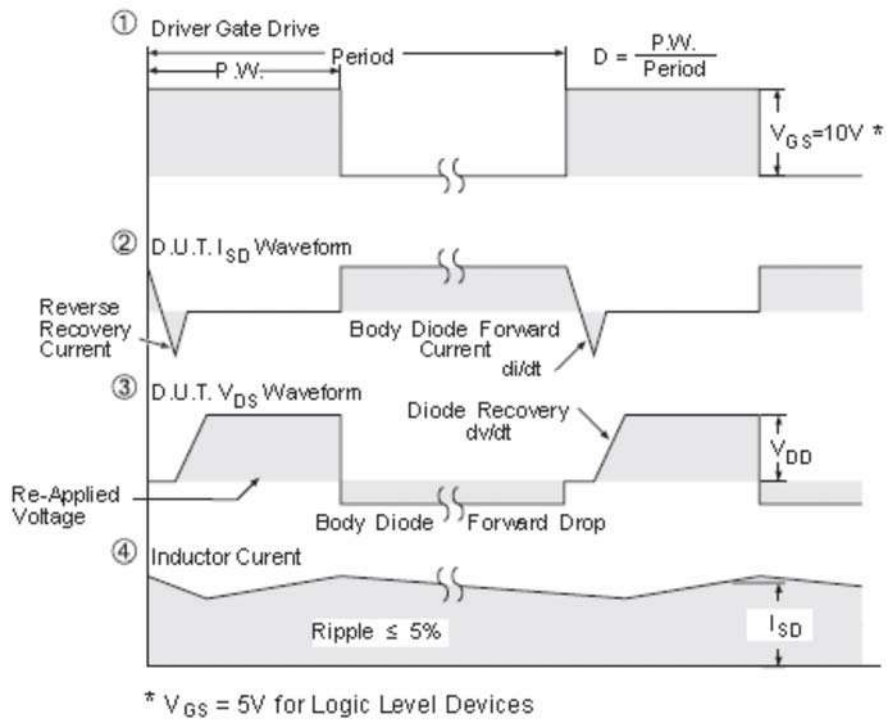
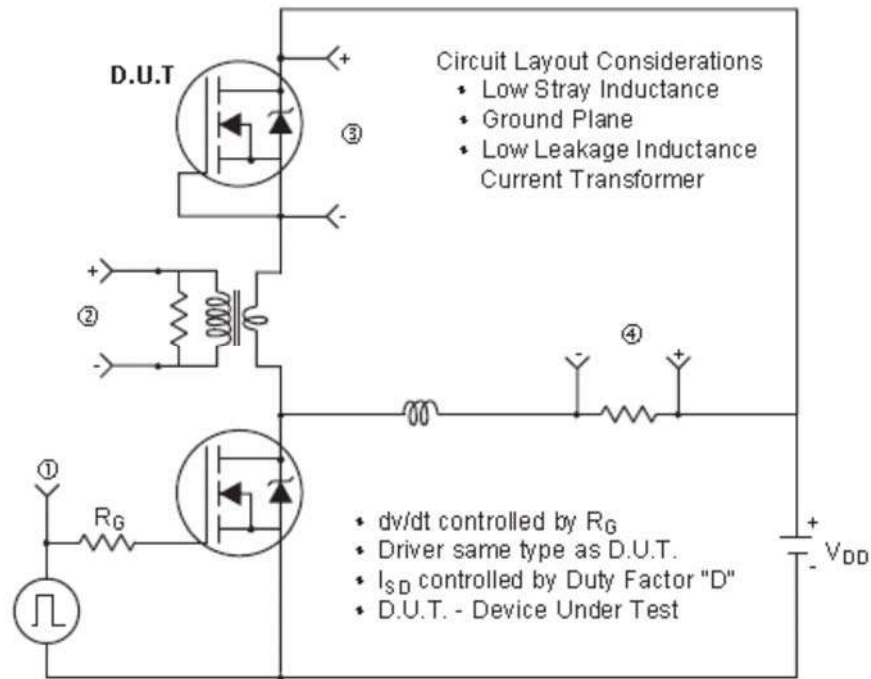
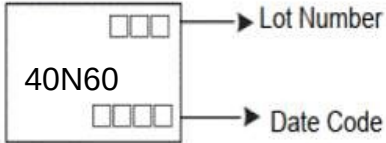


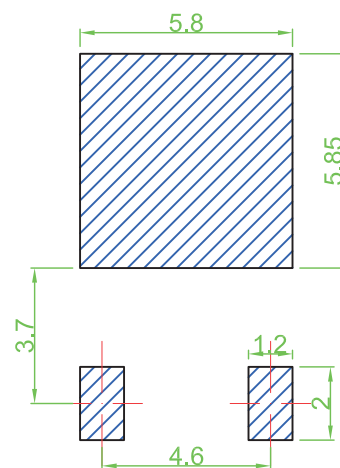
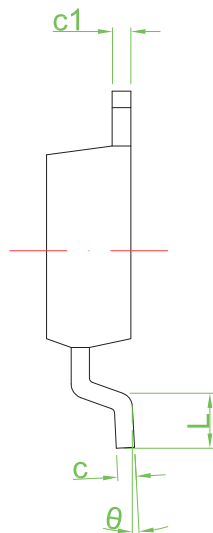
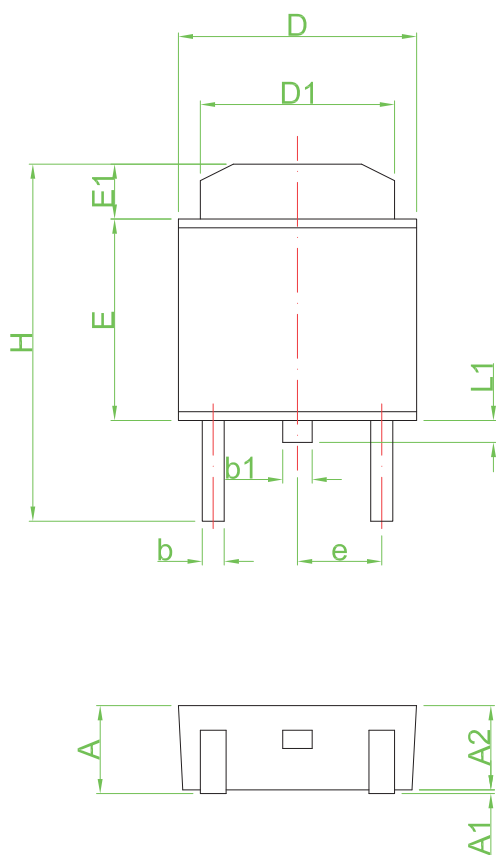
Figure 4: Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
JMD40N60KQ-R	40N60	TO-252	Tape&Reel	2500

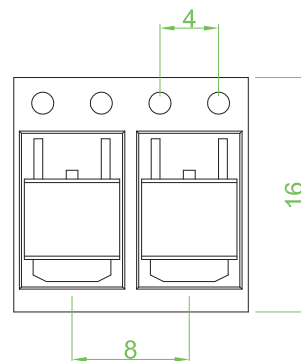
PACKAGE	MARKING
TO-252	 The diagram shows a rectangular marking area for a TO-252 package. It contains the text '40N60' in the center. Above this text are three small squares, with an arrow pointing to the label 'Lot Number'. Below the text are four small squares, with an arrow pointing to the label 'Date Code'.

TO-252 PACKAGE IN FORMATION



Recommended Land Pattern

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.25	2.65	0.089	0.104
A1	0.00	0.15	0.000	0.006
A2	2.20	2.40	0.087	0.094
b	0.50	0.70	0.020	0.028
b1	0.70	0.90	0.028	0.035
c	0.46	0.66	0.018	0.026
c1	0.46	0.66	0.018	0.026
D	6.30	6.70	0.248	0.264
D1	5.20	5.40	0.205	0.213
E	5.30	5.70	0.209	0.224
E1	1.40	1.60	0.055	0.063
H	9.40	9.90	0.370	0.390
e	2.30 TYP		0.09 TYP	
L	1.40	1.77	0.055	0.070
L1	0.50	0.70	0.020	0.028
θ	0°	8°	0°	8°



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